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APPLICATION

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TITLE: IMPROVED SIGNAL ROUTING BETWEEN A MEMORY CONTROL UNIT AND A MEMORY DEVICE

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IMPROVED SIGNAL ROUTING BETWEEN A MEMORY CONTROL UNIT AND A MEMORY DEVICE

Technical Field

The invention relates to signal routing between a memory control unit and a memory extender, such as a memory repeater hub device.

Background

FIG. 1 shows a typical computer system 100. The computer 100 includes a central processing unit (CPU) 105, or processor, and a memory repeater hub 110. A memory control unit (MCU) 120 controls the flow of data into and out of the memory unit 110. The memory unit 110 always includes volatile memory, such as dynamic random access memory (DRAM). The computer also includes other system components, including a non-volatile storage device, such as a hard disk 125, and a modem 130 to connect the computer 100 to a network 135.

The speed at which the computer operates depends in large part on the speed at which data is transferred between the processor 105 and the memory unit 110. One memory architecture in particular, known as the Rambus architecture, is designed to

transfer data to the processor 105 at very high rates, *e.g.*, 1.6 GB/s for a typical Rambus DRAM (RDRAM) module.

FIG. 2 shows a common routing configuration for signal lines connecting the MCU 120 to the memory unit. Each signal line 150 leaves the MCU 120 with a width of approximately 18 mils. Before reaching the appropriate pin 155 on the memory unit, the signal line 150 narrows, or "necks down", to a width of approximately 5 mils. The signal line 160 exiting the pin 155 also has a width of approximately 5 mils before expanding to a width of approximately 18 mils. A ground trace 165 separates the 5 mil neck down portions of the signal lines 150, 160. As a result of this congestion, the signal line 150 into the memory unit and the signal line 160 out of the memory unit often must be formed on different layers of the circuit board on which the MCU and memory unit reside.

Summary

A computer system includes a processor and a multi-layer circuit board having a memory unit, a memory control unit, and a data bus coupling the memory control unit to the memory unit. A first signal line is formed on a selected layer of the circuit

board and connected between a first pin on the memory repeater hub and the memory control unit. A second signal line is also formed on the selected layer of the circuit board and is connected to the first pin on the memory unit.

Other embodiments and advantages will become apparent from the description and claims that follow.

Description of the Drawings

FIG. 1 is a block diagram of a computer system.

FIG. 2 is a schematic diagram of a conventional signal routing scheme.

FIG. 3 is a schematic diagram of an improved signal routing scheme.

FIG. 4 is a cross-sectional view of a multi-layer circuit board having signal lines routed according to the scheme of FIG. 3.

Detailed Description

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FIG. 3 shows a signal routing configuration that reduces the area required for each signal line 200 running between the MCU 120 and the memory unit. In this configuration, the signal line 200 has a width of approximately 18 mils with a 5 mil neck

down portion 205 contacting the corresponding pin 135 on the memory unit. The signal line 210 exiting the pin 135 also has a width of approximately 18 mils with a 5 mil neck down portion 215 contacting the pin 135. The two neck down portions 205, 215 run substantially parallel to each other for a distance, and then act an acute angle for another distance, the portions are separated by a gap 220. This gap 220 also has a width of approximately 5 mils. The neck down portions 205, 215 are not separated by a ground trace.

The gap 220 between the neck down portions 205, 215 provides the isolation between the signal lines 200, 210 yet reduces the area required to route the signal lines on a circuit board. Placing the gap 220, and not a ground trace, between the neck down portions 205, 215 can reduce congestion at the memory unit. This allows the signal lines 200, 210 into and out of the memory unit to be routed on a single layer of the circuit board on which the MCU and the memory unit reside. Routing the signal lines in this manner reduces the number of layers required to route signals between the MCU and the memory unit by a factor of two. As a result, the circuit board on which the MCU and memory unit reside can be less expensive to produce than conventional memory boards.

FIG. 4 shows the neck down portions 205, 215 of the signal line 200 on a multi-layer circuit board 225. The neck down portions 205, 215 into and out of the memory unit are formed on a single layer of the circuit board 225 and are separated by a gap 220 in which no traces are formed. No ground trace lies between the signal lines 205, 215. In some embodiments, ground traces 230, 235 lie on either side of the signal lines 205, 215 on the same layer of the circuit board 225. A ground plane 240 lies above or below the signal lines 205, 215 on another layer of the circuit board.

A number of embodiments have been described. Nevertheless, one of ordinary skill will understand that variations are possible. For example, while the invention has been described in terms of signal routing to a Rambus device, this scheme is useful in routing signals to other types of memory devices and even to other system components. Accordingly, other embodiments are within the scope of the following claims.